



(integrated circuit) and (memory controller) and

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CPU, memory controller, bus bridge integrated circuits, layout structures ...

US Pat. 5784291 - Filed Aug 29, 1996 - Texas Instruments, Incorporated

Bus 714 is connected to **CPU** 701, to a bus bridge **circuit** 716, and to a **DRAM memory controller** (MCU) 718. Registers 712 also are bidirectionally connected to ...

RAM controller interface device for RAM compatibility (memory translator hub)

US Pat. 6449679 - Filed Feb 26, 1999 - Micron Technology, Inc.

A synchronous **DRAM** system, in contrast, can use four 1 30 ... Each **memory** module would have an **integrated circuit** interface chip which allows the **memory** ...

Integrated circuits for low power dissipation in signaling between different ...

US Pat. 5652370 - Filed Oct 9, 1996 - Texas Instruments Incorporated

Bus 714 is connected to **CPU** 701, to a bus bridge **circuit** 716, and to a **DRAM memory controller** 10 25 40 14 (MCU) 718. Registers 712 also are bidirectionally ...

Bus quieting circuits, systems and methods

US Pat. 5666497 - Filed Oct 3, 1996 - Texas Instruments Incorporated

Bus 714 is connected to **CPU** 701, to a latter two chips can even be pinned out in a preferred bus bridge **circuit** 716, and to a **DRAM memory controller** ...

Integrated circuit device with a memory that preserves its content ...

US Pat. 5872903 - Filed Feb 24, 1997 - Mitsubishi Denki Kabushiki Kaisha

1, the **CPU** 1 and the **DRAM** 2 are **integrated** on a chip T. An outline of the ...

The **CPU** 1, the **DRAM** 2, a buffer 4, a **memory controller** (MC) 5 and the cache 6 ...

Integrated circuit design for handling of system management interrupts (SMI ...

[US Pat. 5624997 - Filed Sep 18, 1996 - Texas Instruments Incorporated](#)

Bus 714 is connected to **CPU 701**, to a convenience. bus bridge **circuit 716**, and to a **DRAM memory controller** In the three-chip embodiment illustrated in FIGS. ...

[Bus bridge device including data bus of first width for a first processor ...](#)

[US Pat. 5909559 - Filed Apr 4, 1997 - Texas Instruments Incorporated](#)

DRAM memory controller MCU supports up to 256 megabytes or more of **DRAM memory**

... in 60 65 are described various improved **integrated circuit** embodiments, ...

[Processing system with separate general purpose execution unit and data ...](#)

[US Pat. 6658552 - Filed Oct 23, 1998 - Micron Technology, Inc.](#)

4 is a block diagram of a **memory controller circuit** for receiving and performing

... and a second data cache and main **DRAM memory** external to the processor. ...

[Systems, circuits and methods for mixed voltages and programmable voltage ...](#)

[US Pat. 5734919 - Filed Aug 29, 1996 - Texas Instruments Incorporated](#)

CPU core DRAM memory controller 718 supports up to 256 mega- 702 is described in

... Bus bridge 716 advantageously acts, for **integrated circuit** having clock ...

[Main memory arbitration with priority scheduling capability including ...](#)

[US Pat. 5781927 - Filed Jan 30, 1996 - United Microelectronics Corporation](#)

If the **CPU 110** is in urgent need for the **DRAM 140**, the main **memory** ... and the

data buffer **controller 130**, can be combined into a single **integrated circuit**, ...

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